# Ovonics Unified Memory-- A High Performance Nonvolatile Memory Technology for Stand Alone Memory and Embedded Applications

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# Agenda

- Comparison of Memory Technologies
- OUM Technology Concept
- Memory Cell Characteristics
- 4Mb Test Chip
- Memory Array Characteristics
- Technology Challenges
- Summary

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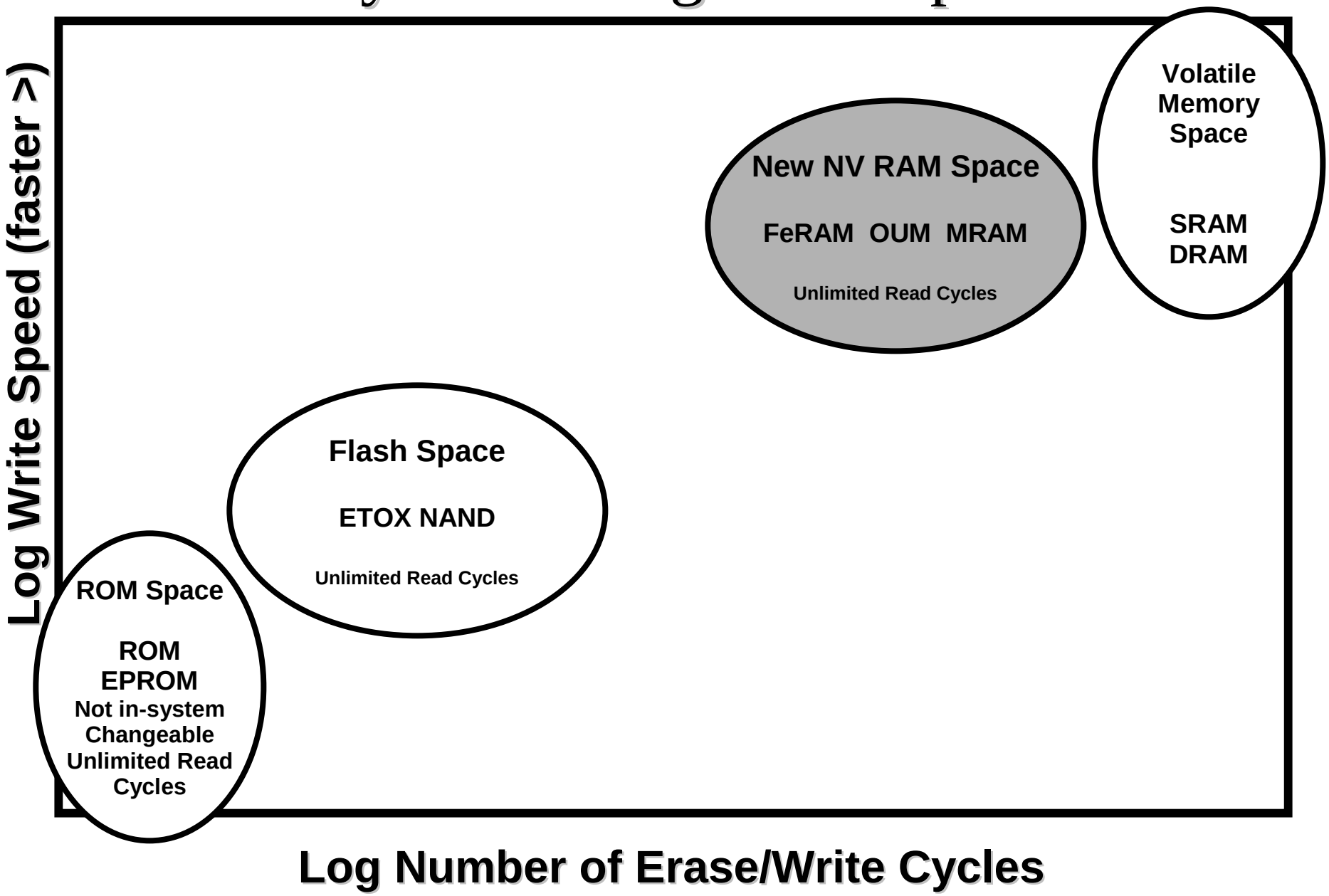
# Memory Technologies Comparison



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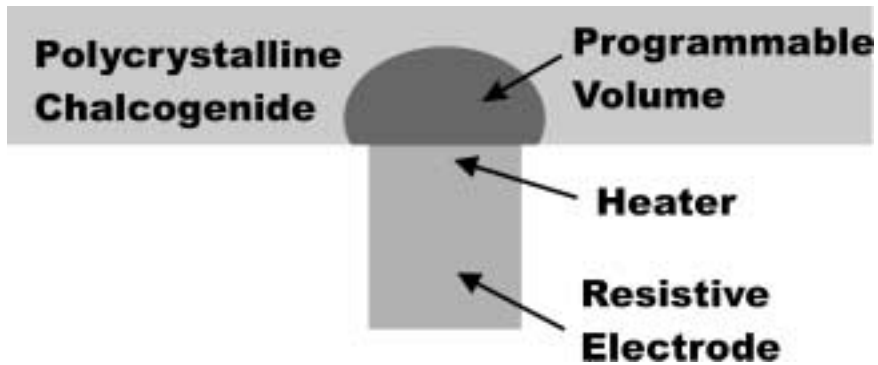
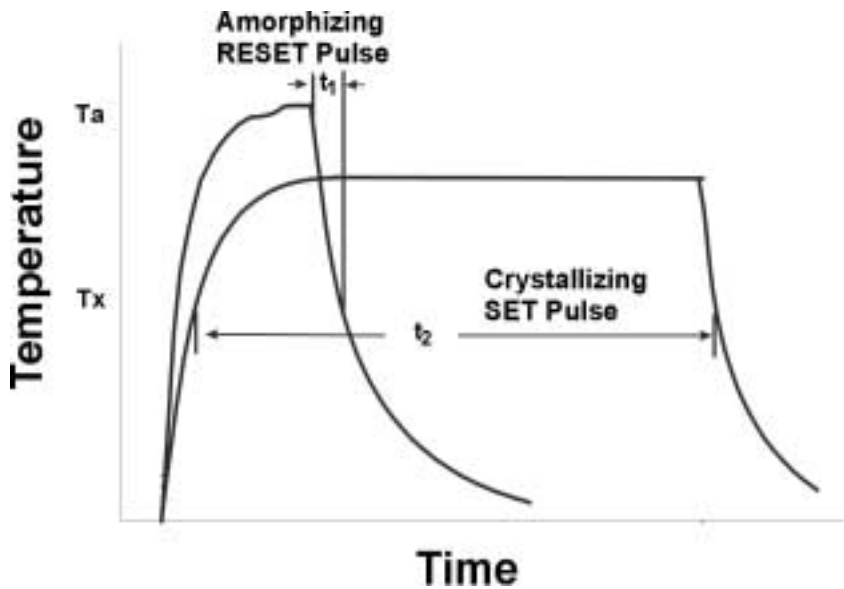
# OUM Concept

- Operation
  - Chalcogenide material alloys used in re-writable CDs and DVDs
  - Electrical energy (heat) converts the material between crystalline (conductive) and amorphous (resistive) phases
  - Cell read by measuring resistance

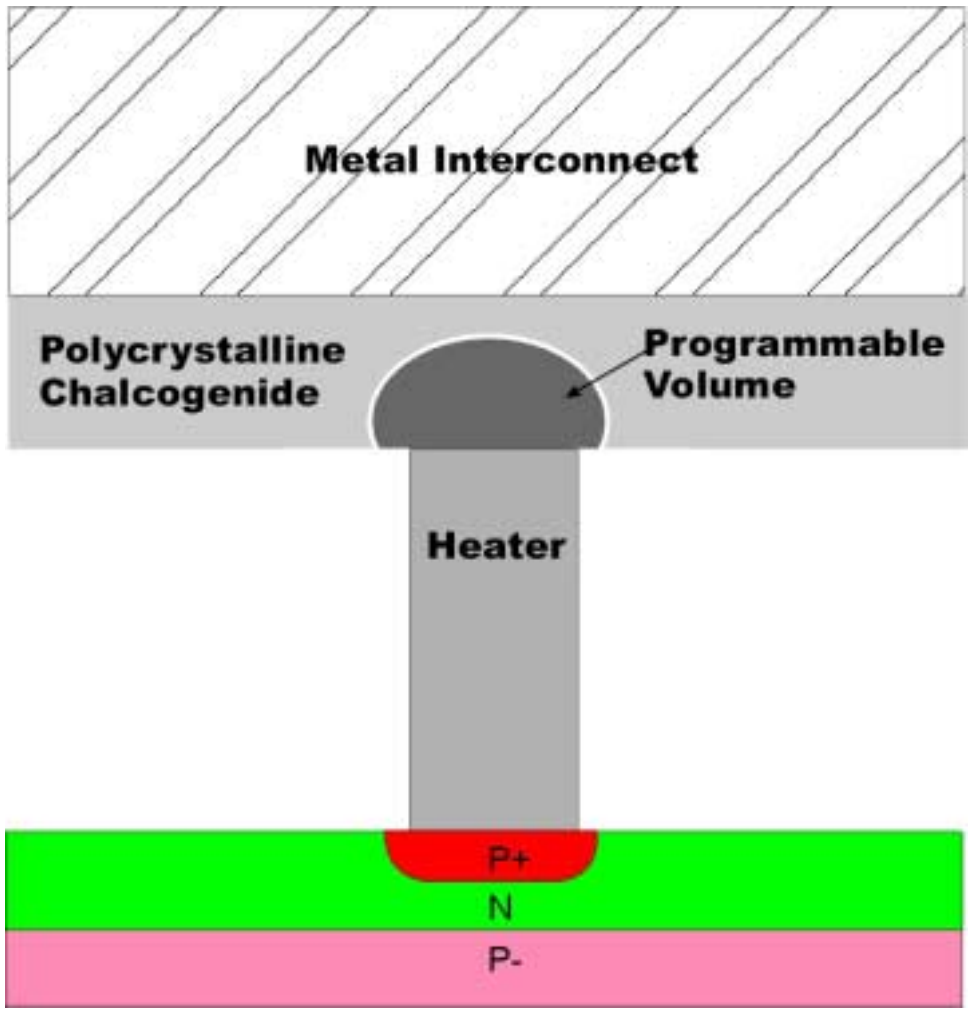
Data Storage Region

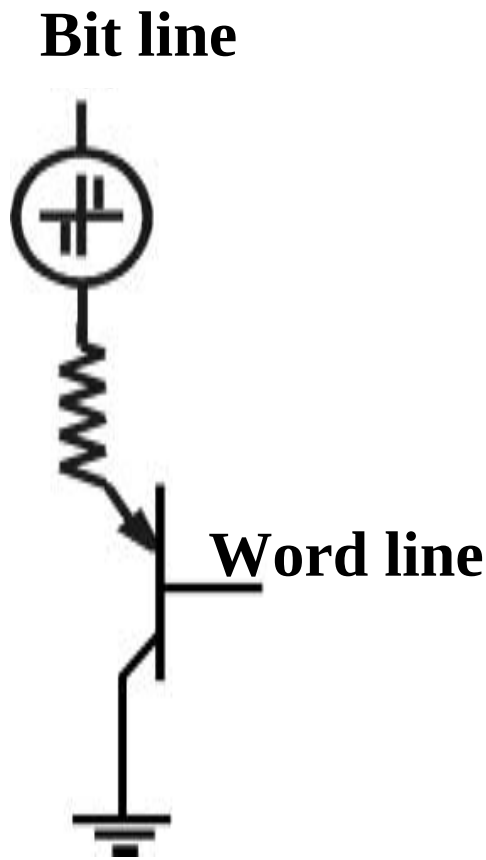


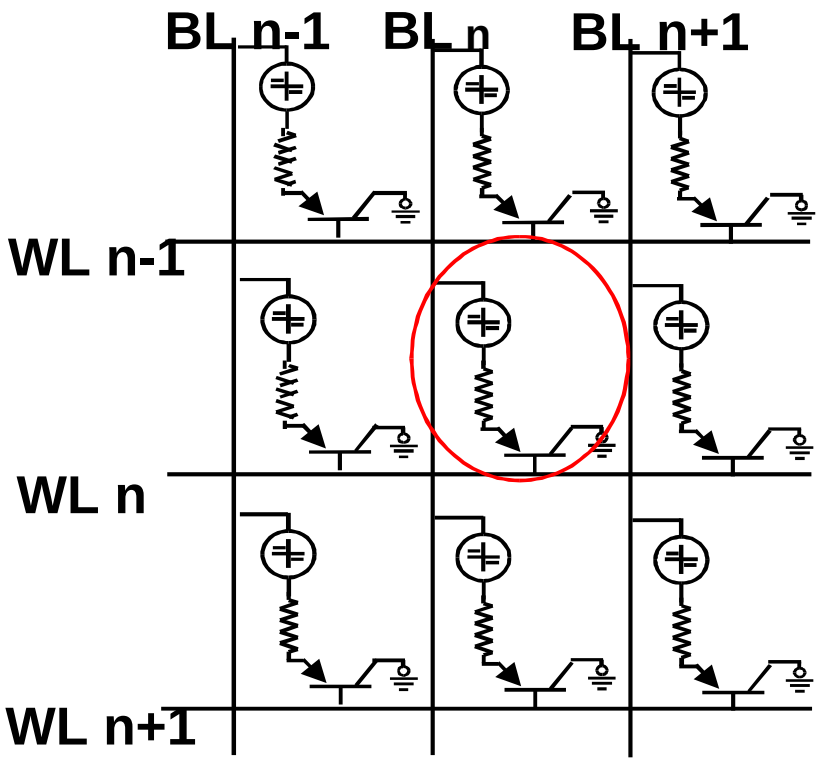

- Attributes
  - Non-volatile, Direct overwrite
  - High density
  - Non-destructive read
  - Low voltage and low power
  - ~1E12 write/Erase cycles
  - Easy to integrate w/ logic

# Array Element: Junction Diode selection



# Memory array operation showing select and deselect conditions




| | Reset | Set | Read |
|---|---|---|---|
| BLn | Ireset | Iset | Iread |
| BLn-1 | 0V | 0V | 0V |
| BLn+1 | 0V | 0V | 0V |
| WLn | 0V | 0V | 0V |
| WLn-1 | Vdd | Vdd | Vdd |
| WLn+1 | Vdd | Vdd | Vdd |

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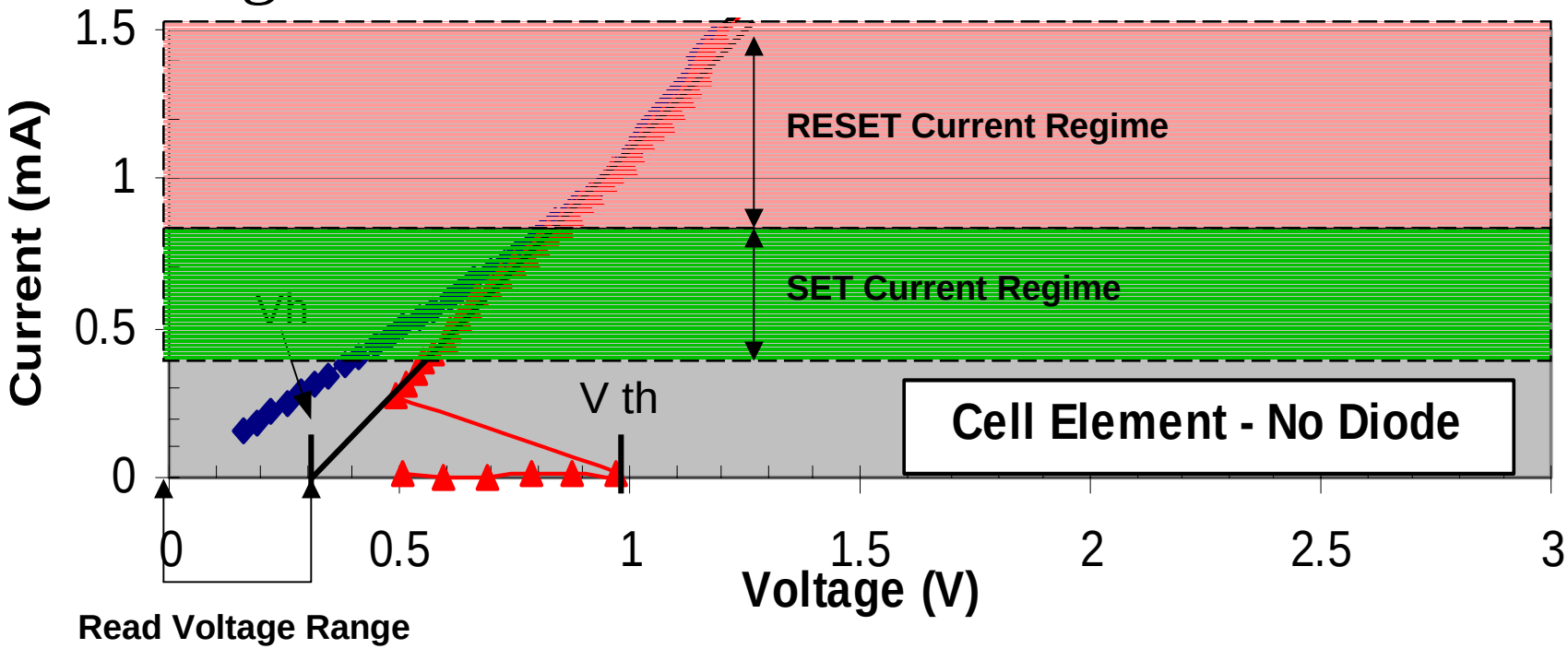
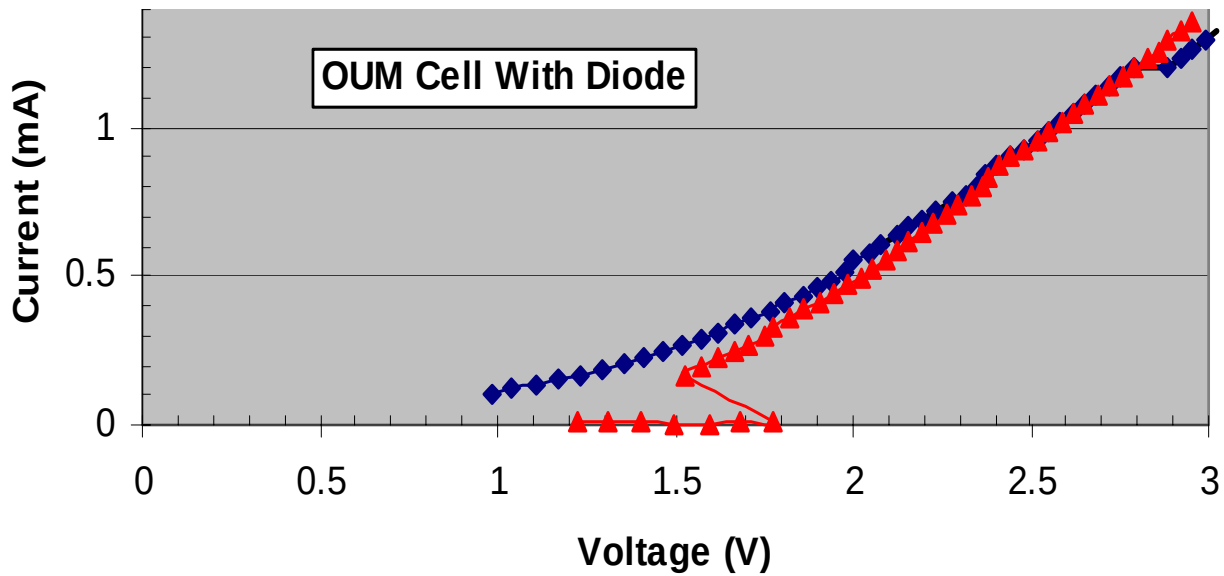
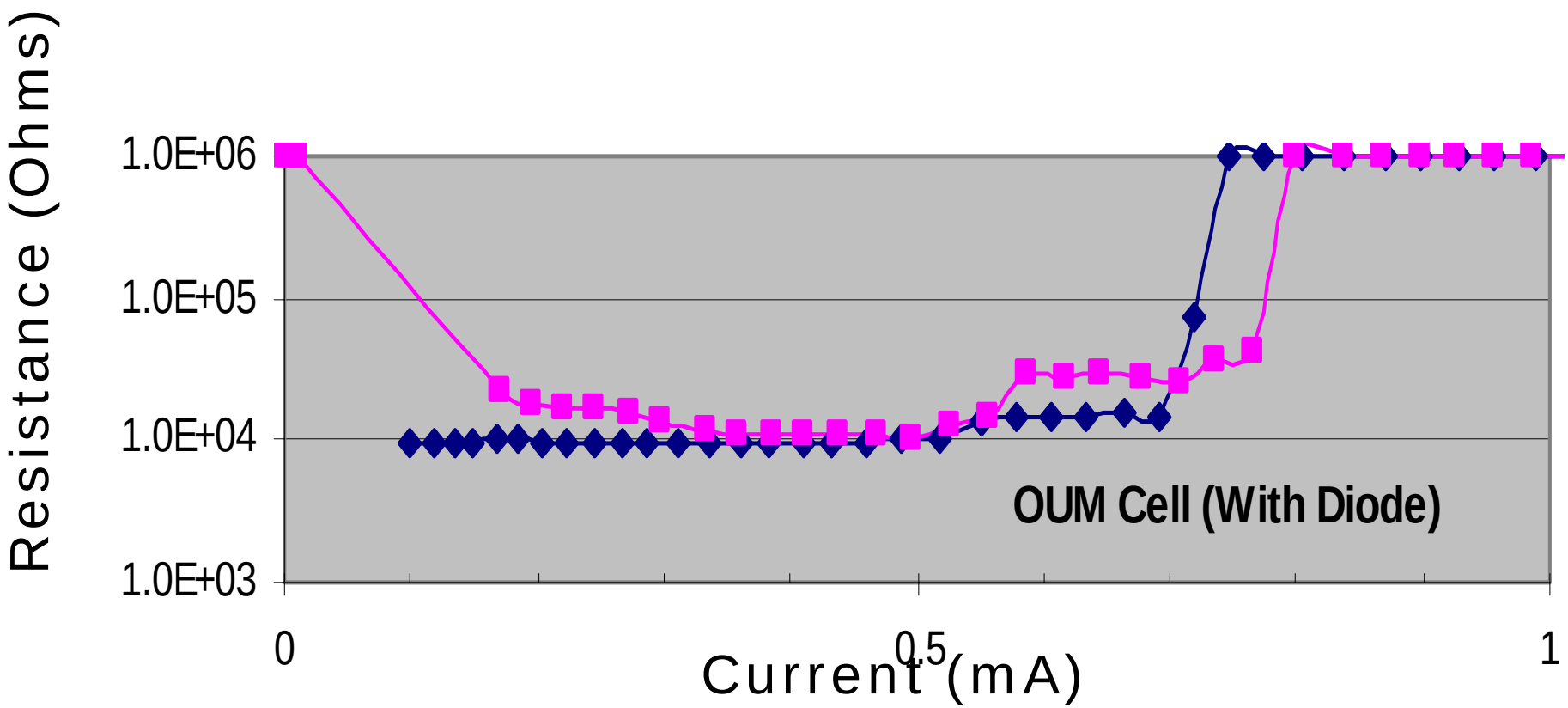
# Single Cell IV Curves with and without diode

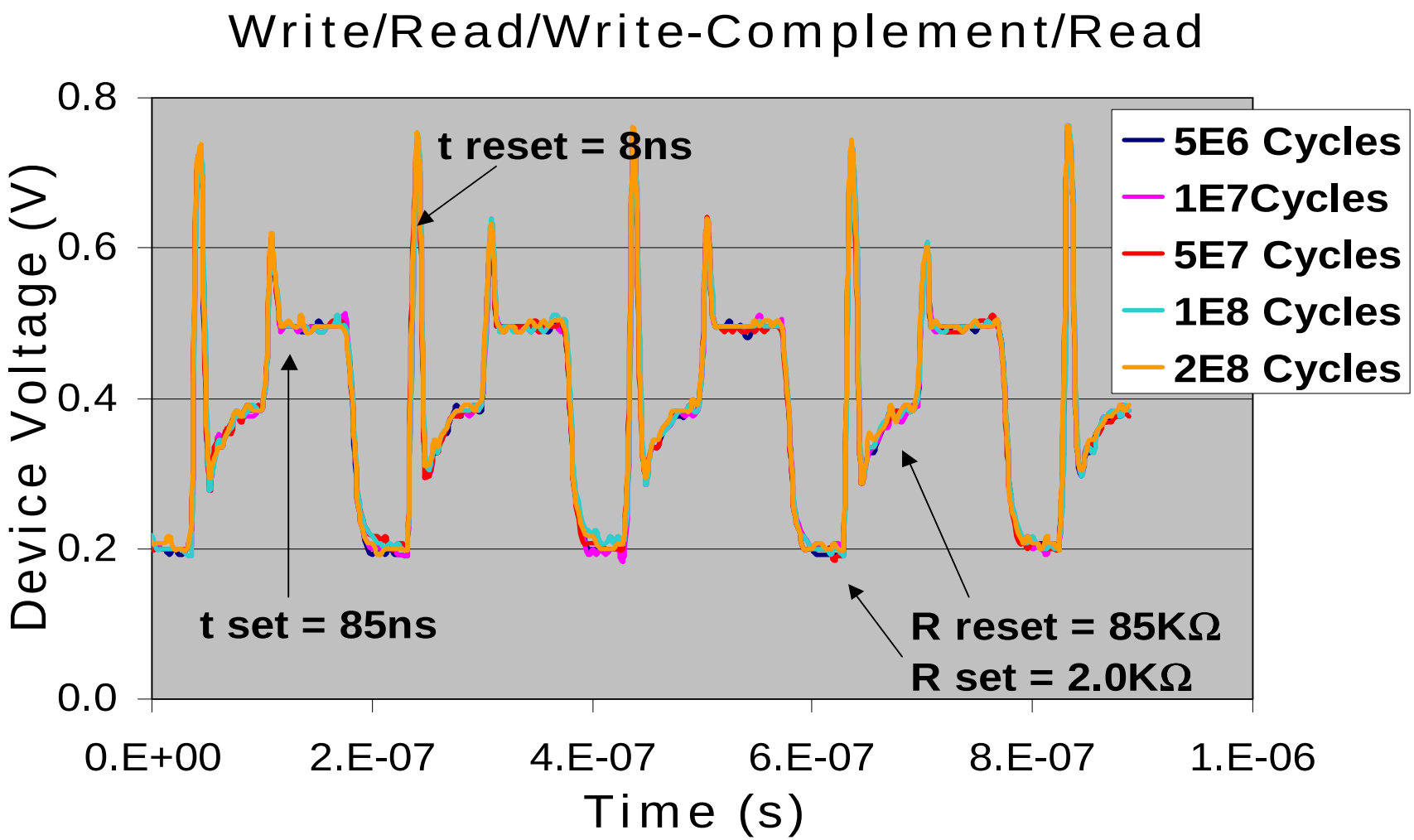


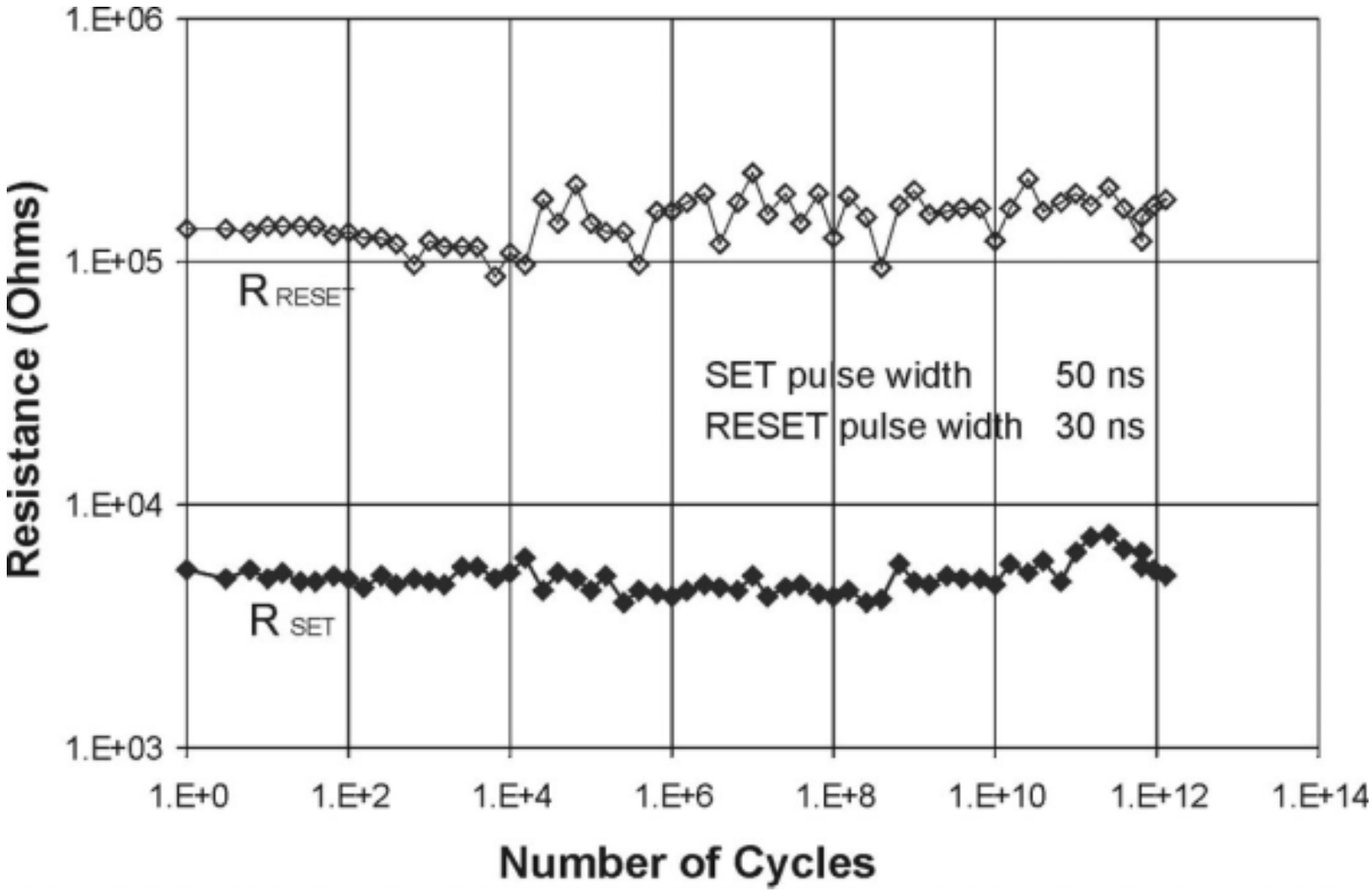
# Cell Programming RI Characteristics



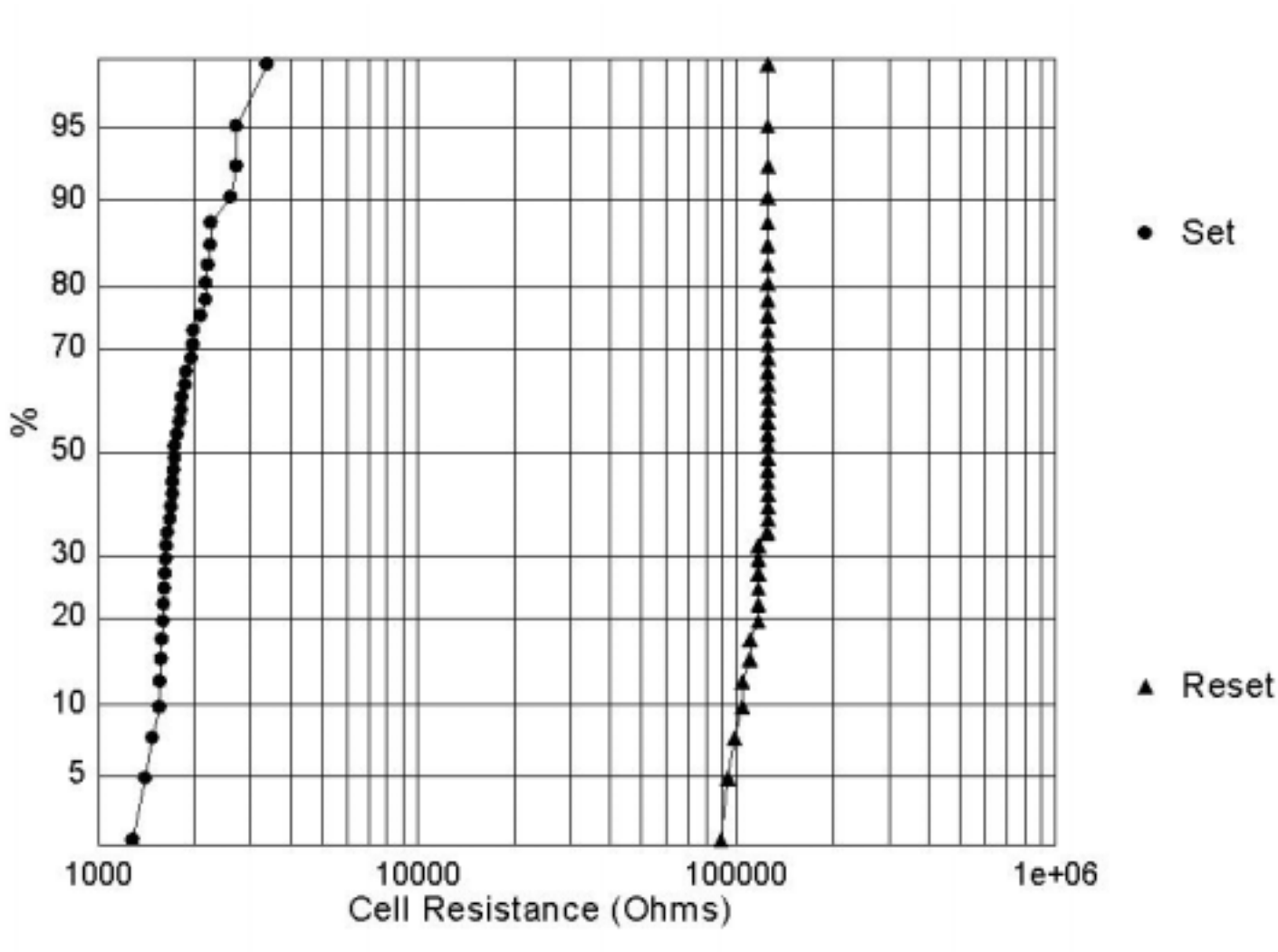
# Direct Write of Phase Change Element at 5MHz



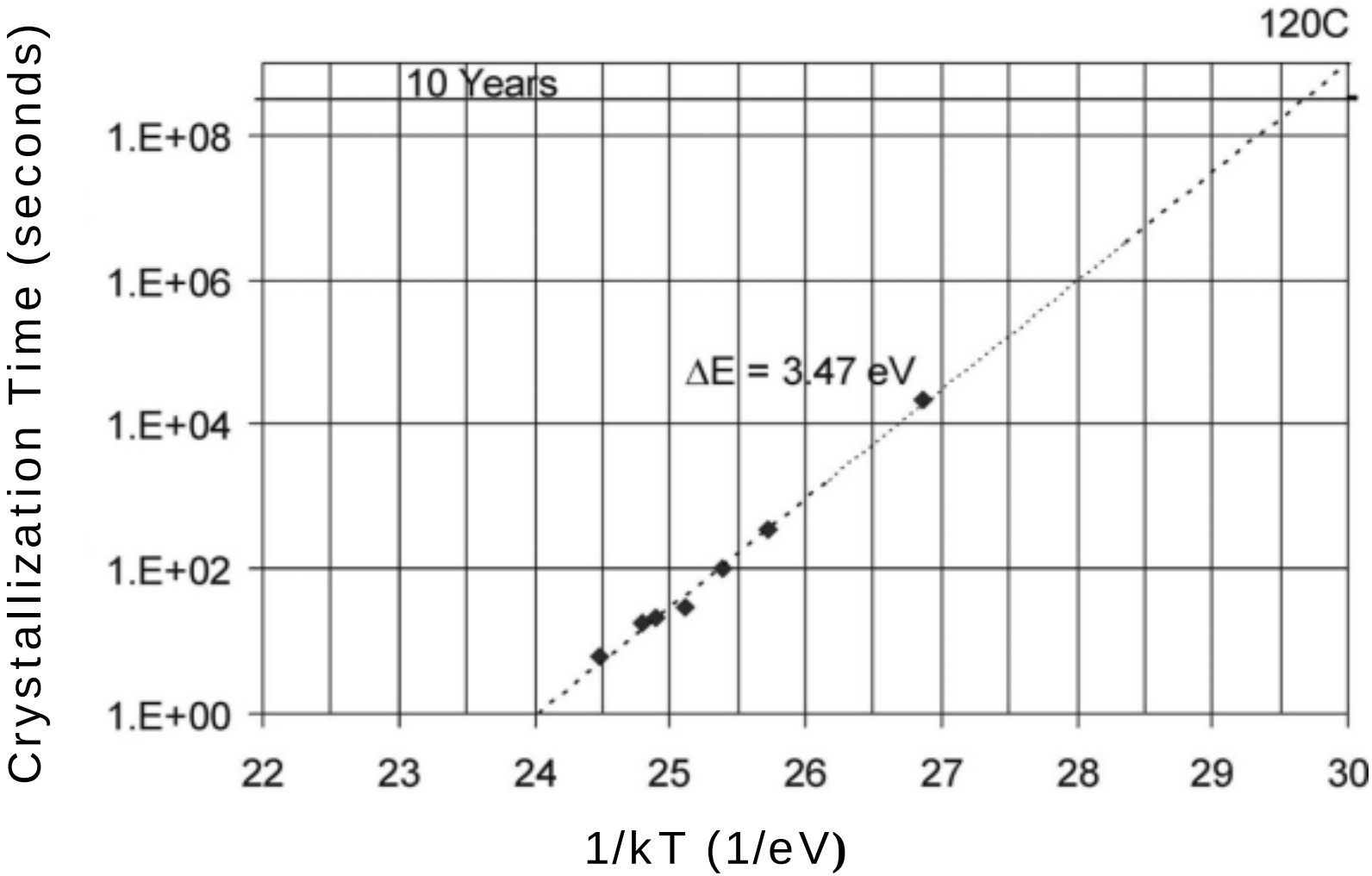
# $R_{set}$ and $R_{reset}$ as Function of Cycles



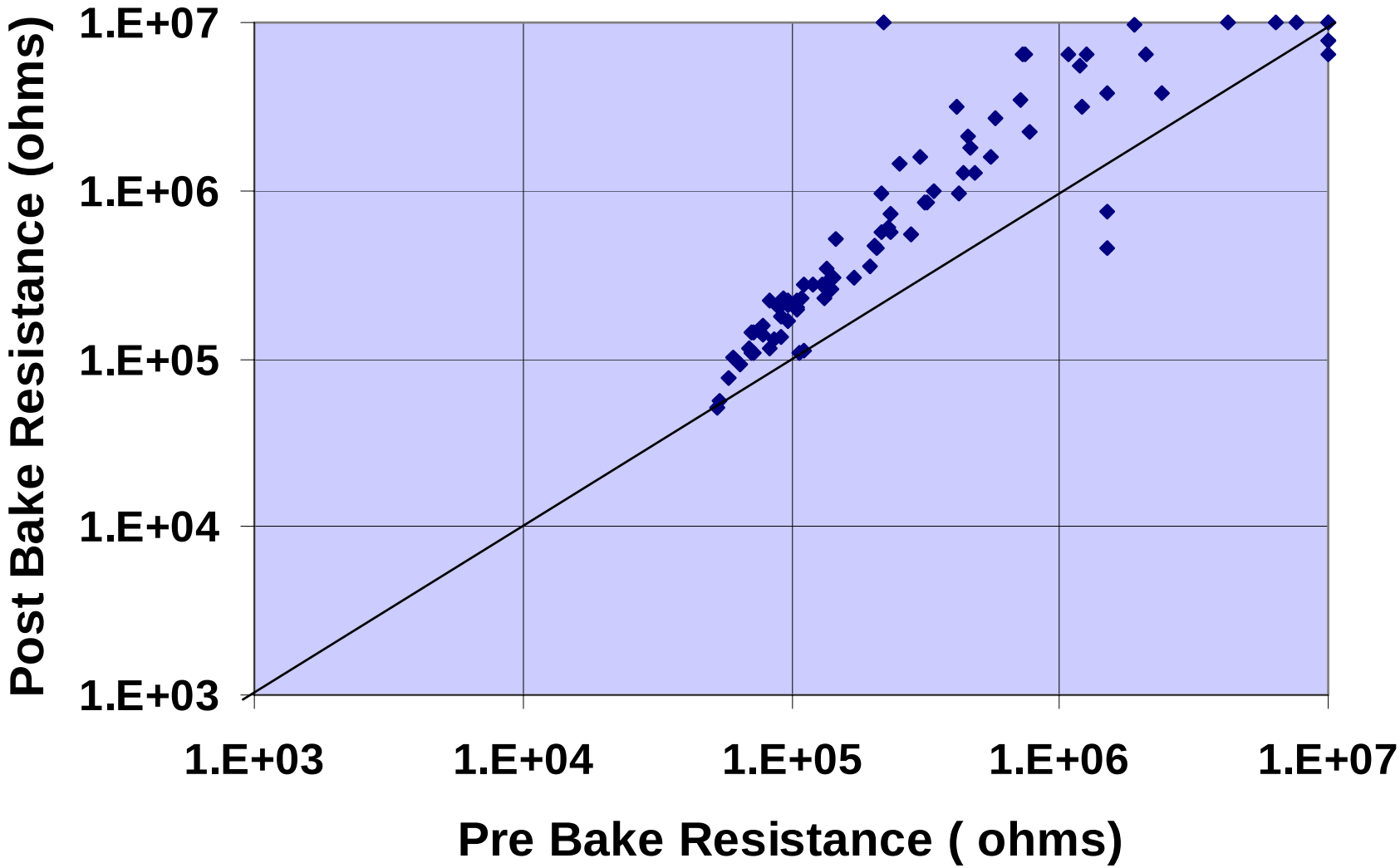
# $R_{set}$ and $R_{reset}$ Distribution after $10^7$ Cycles



# Intrinsic Retention Characteristics



# Data Retention 140°C, 16 Hours Bake



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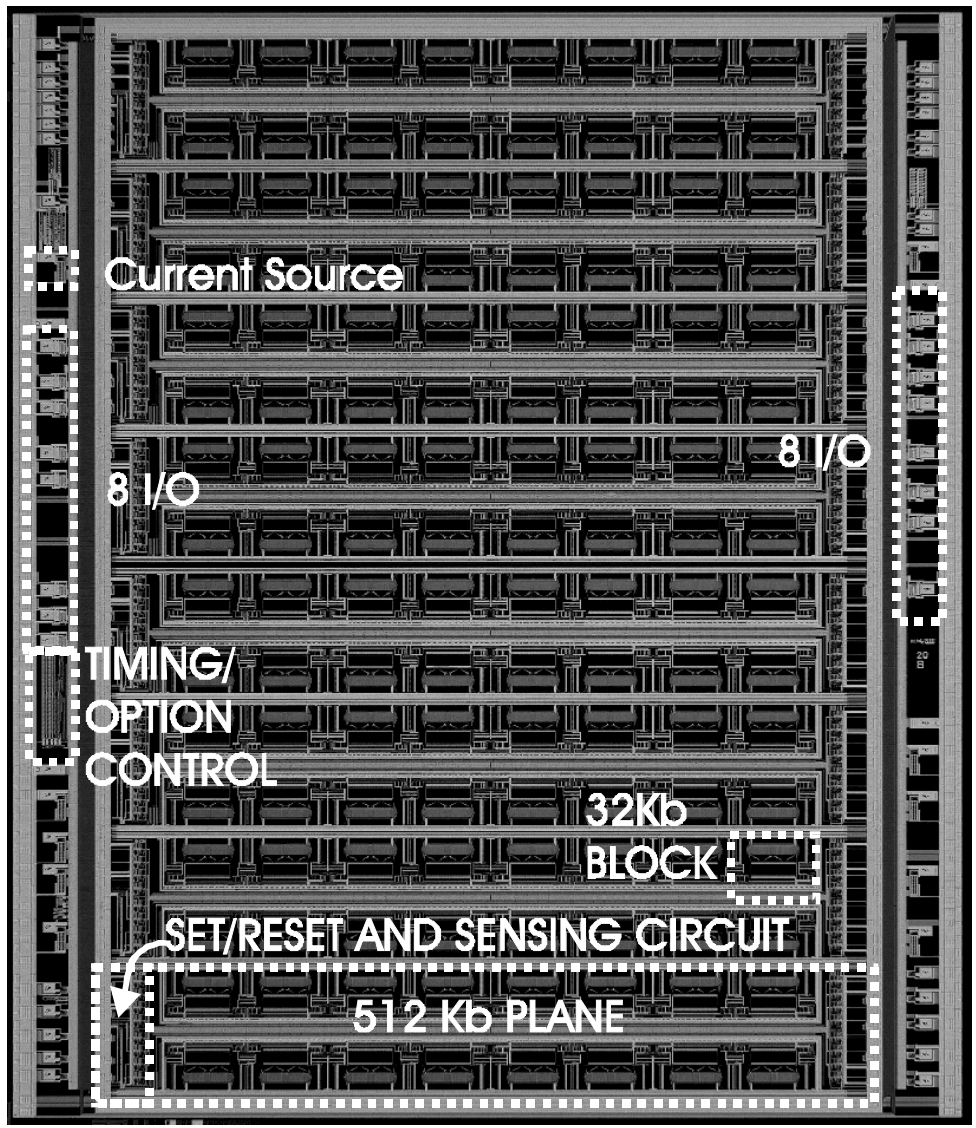
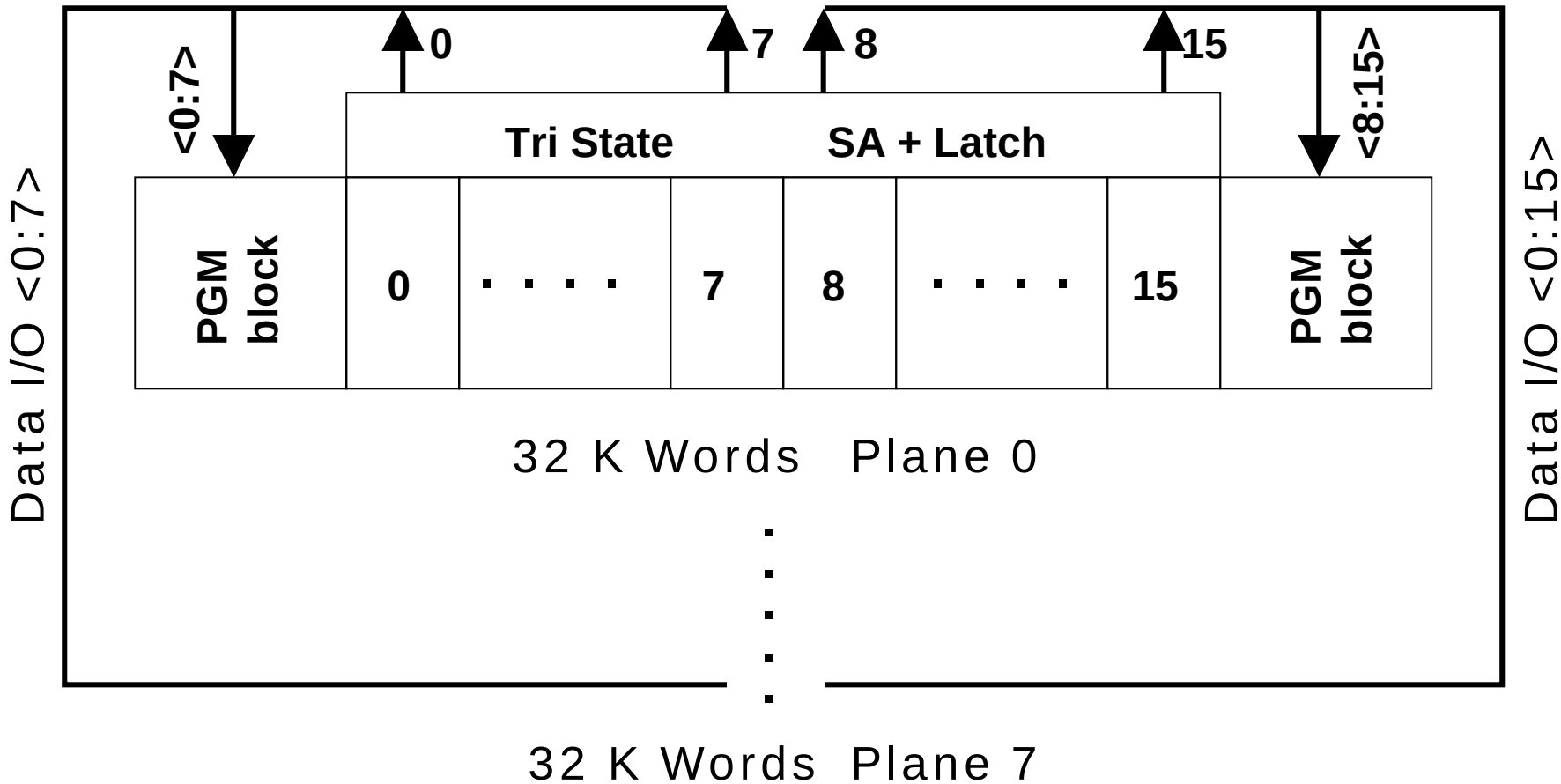
# 4M Test Vehicle Device Parameters

- Min. litho feature 0.18 μm
- Process Single polycide, single metal, twin well CMOS
- Cell Size 7.7 $\lambda^2$
- CMOS transistors 3.3 V
- CMOS gate oxide 8 nm
- Memory material $Ge_xSb_yTe_z$ alloy
- Power supply 3.3V
- Memory contact size 0.24 μm x 0.24 μm

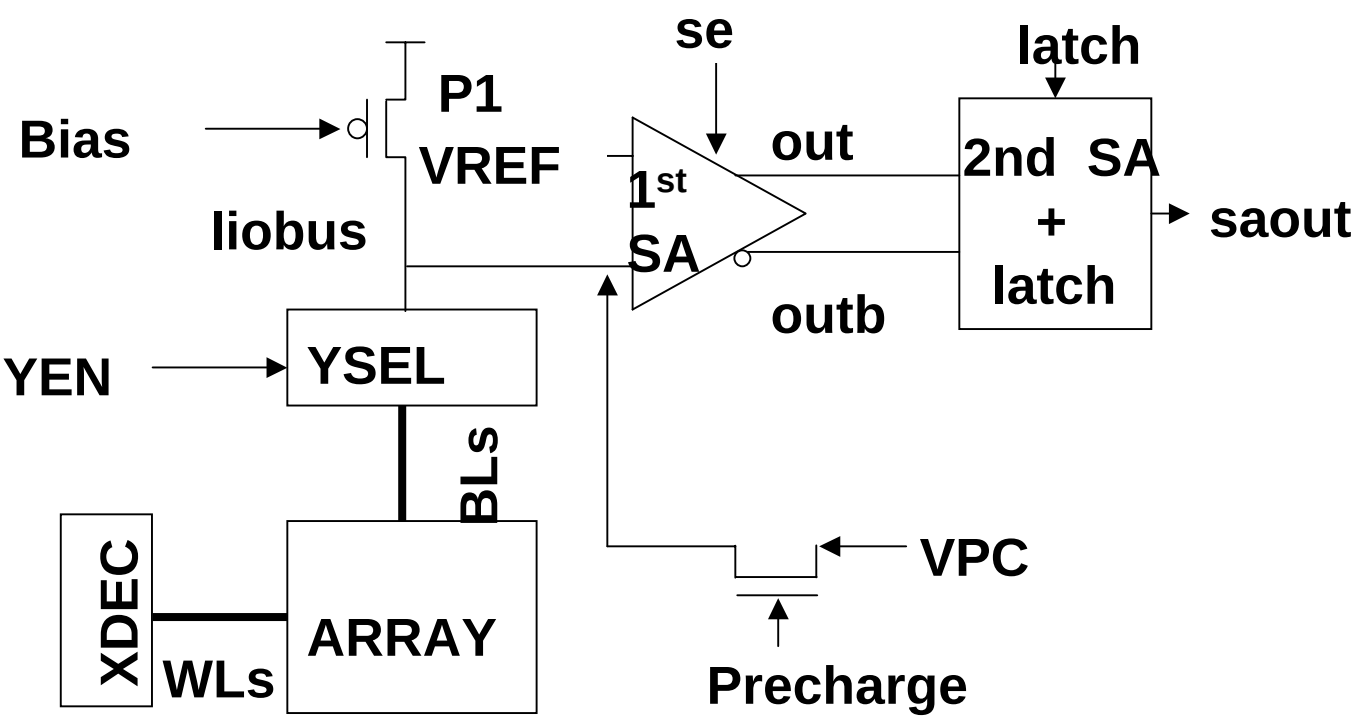
# Photomicrograph of 4 Mb test memory



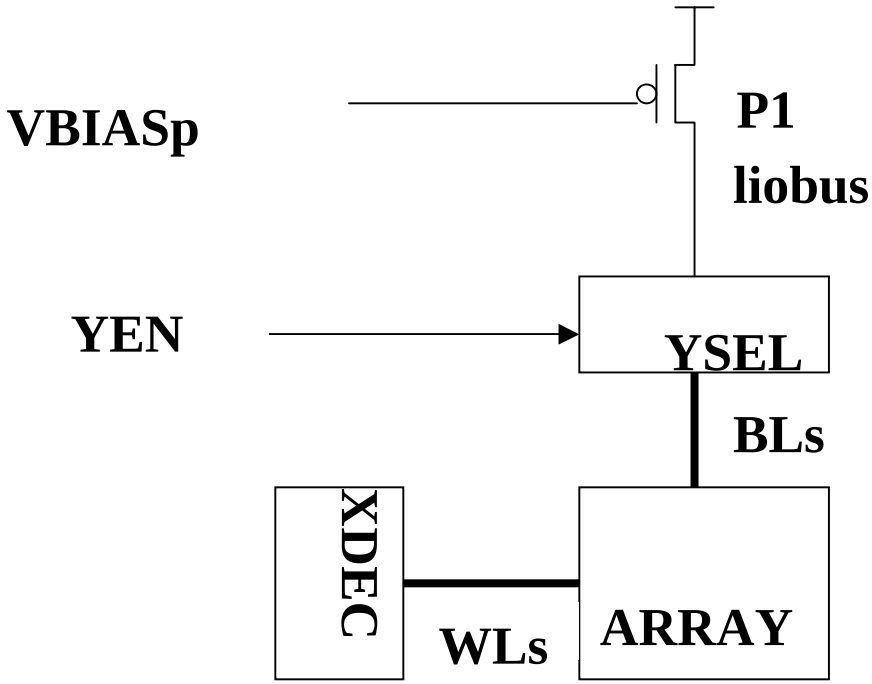
# Array Architecture



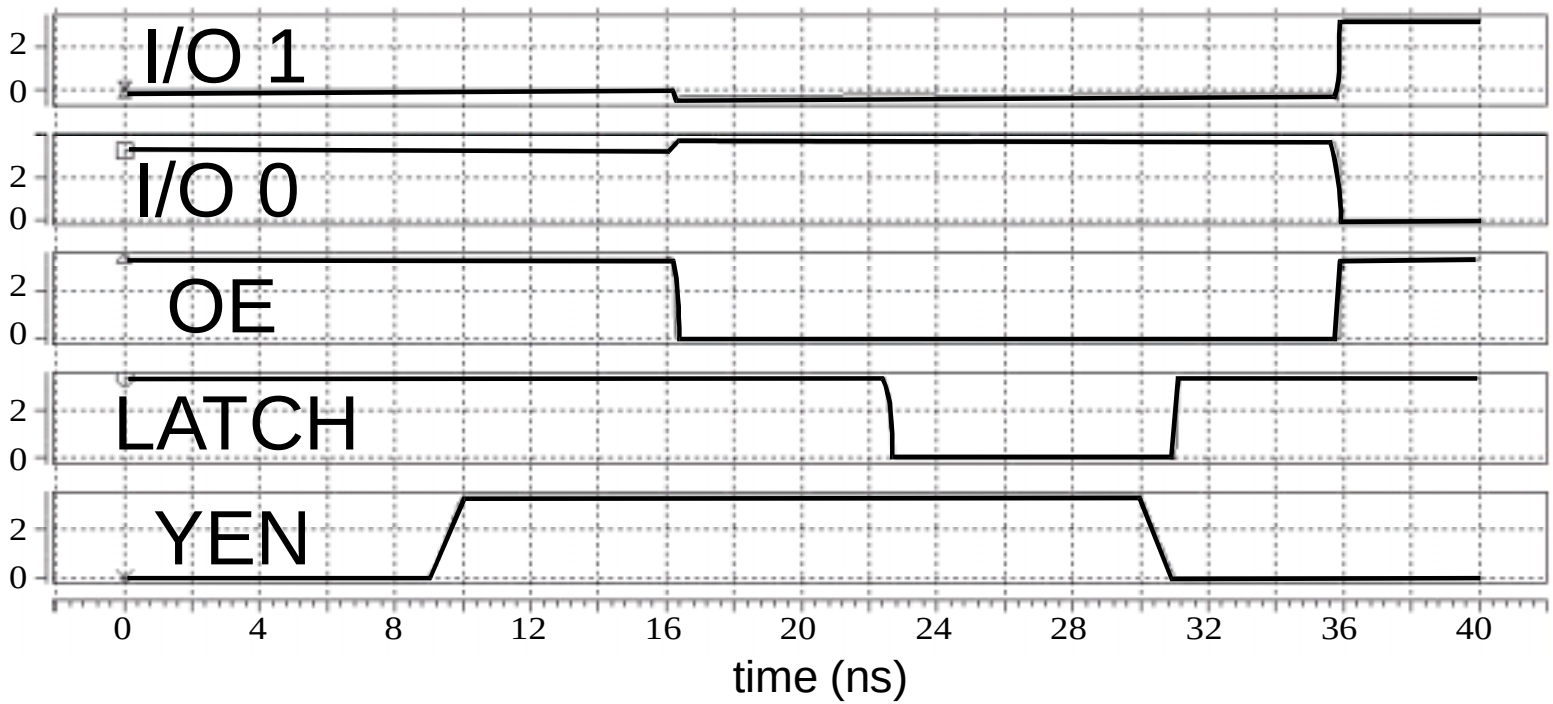
# Read Path Schematic



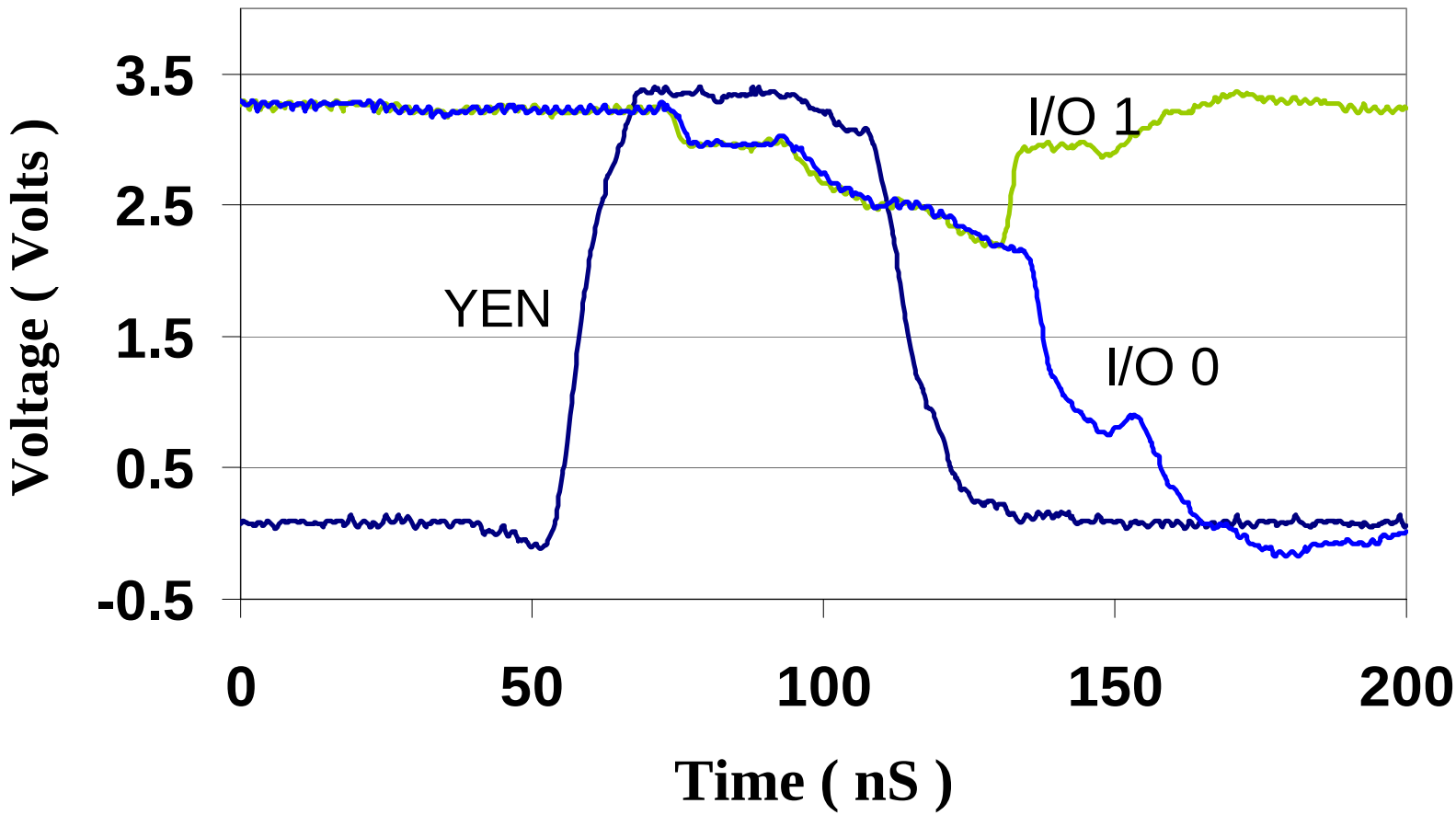
# Write Path Schematic



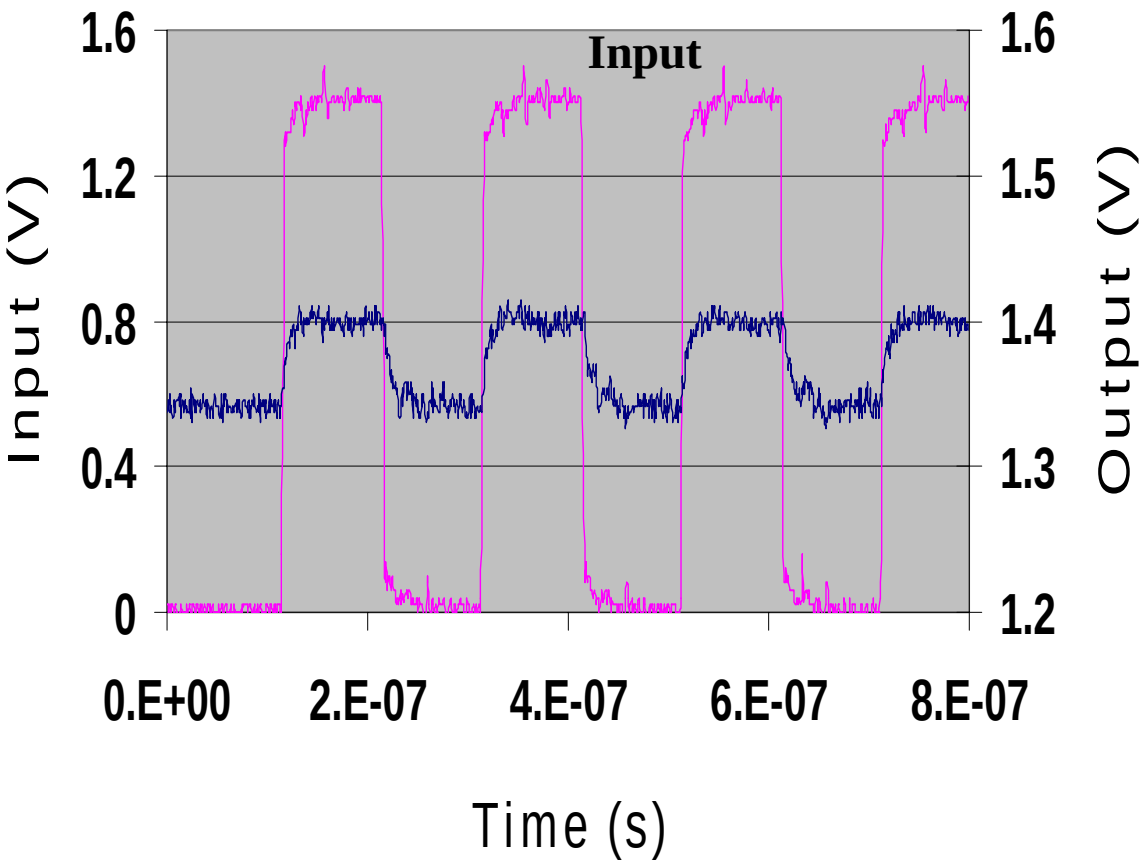
# Data path simulation

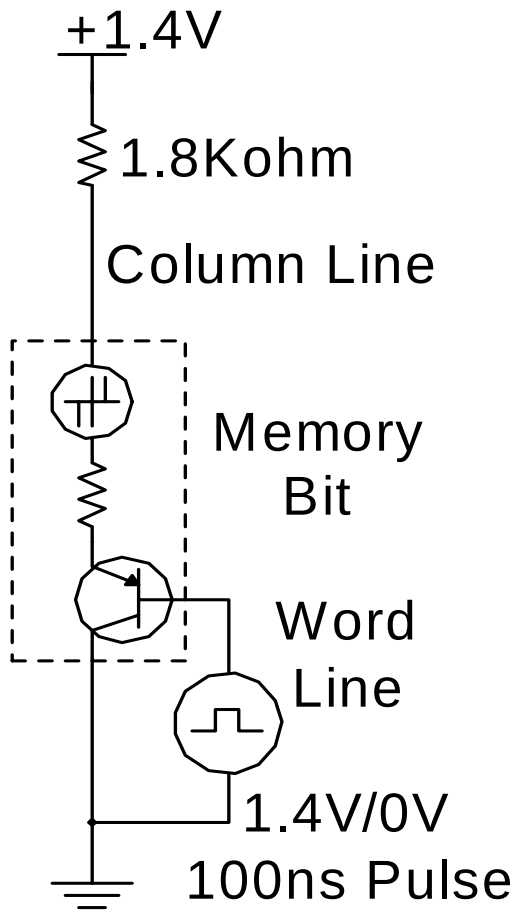


# Data Path Measured Waveform



# Read Cell Select/Deselect Through Word-line PNP



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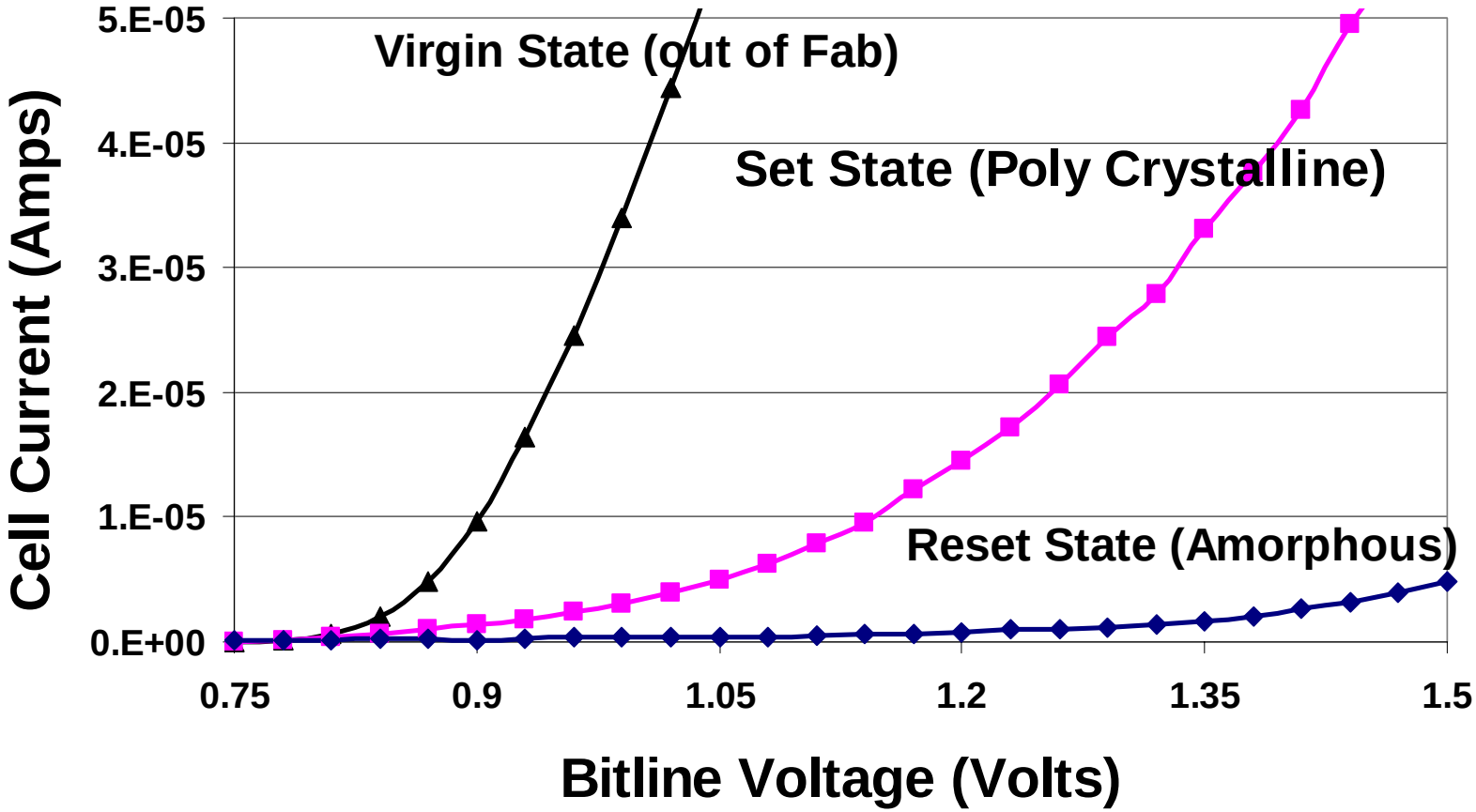
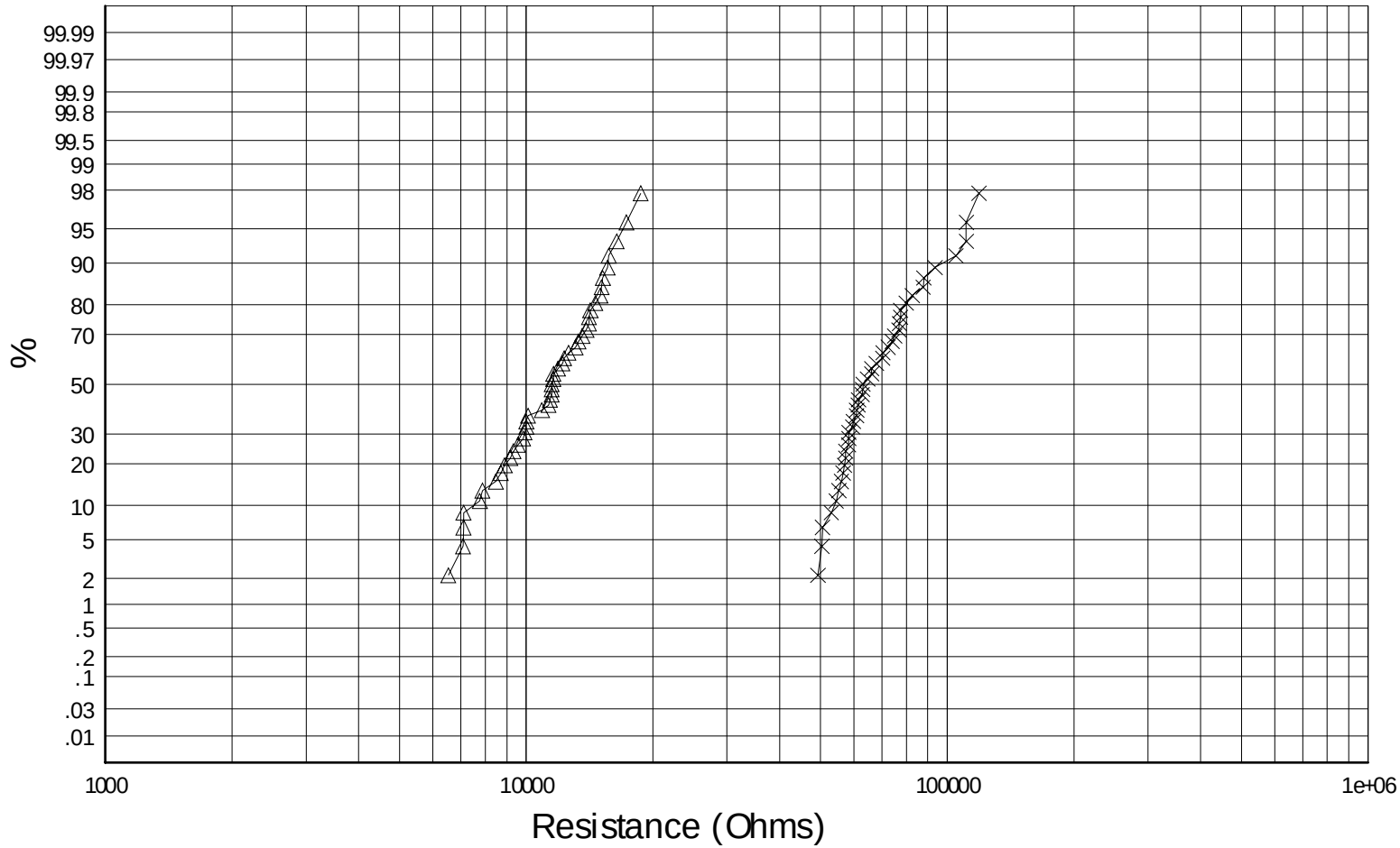
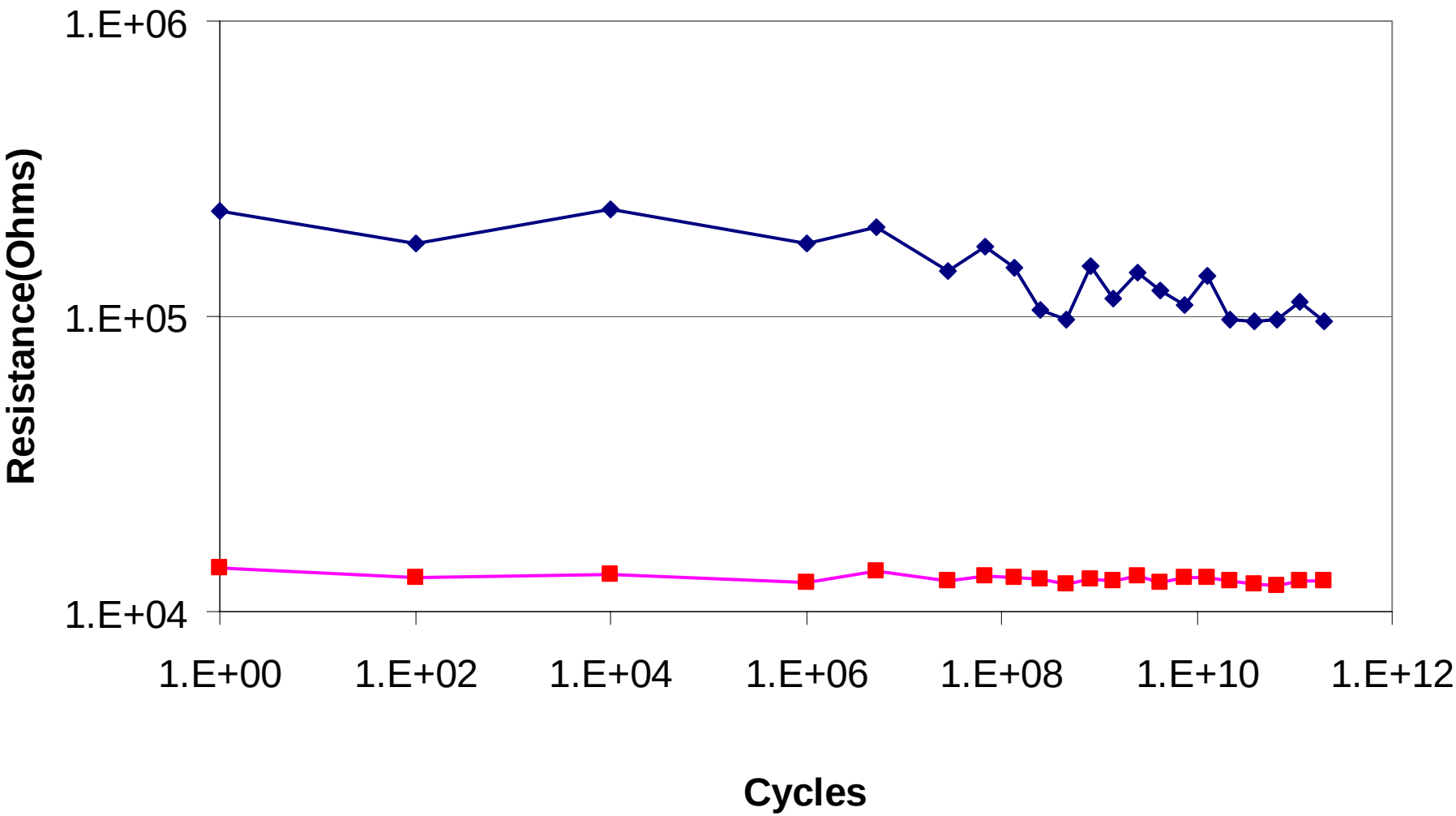
# Array Cell I-V



# Set and Reset Resistance Distribution in Array



# Cycling Performance of Array



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# Technology Challenges

- Reduction of programming current for lower voltage and lower power operation
- Increased set/reset resistance and decreased read current/set current margin with scaling -> impact on read performance/margin
- Management of proximity heating with declining cell space -> disturb risk

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# Summary

- Functional Ovonics Unified Memory Array has been demonstrated in a 0.18 μm integrated CMOS logic process
- Use of diode as a selection device demonstrated with no disturb observed, giving a small and scalable unit memory cell
- Endurance demonstrated to $10^{12}$ set-reset cycles
- Direct 3.3V operation without the use of an on-chip charge pump
- This technology offers the potential of easy addition of nonvolatile memory to a standard CMOS process, is low cost and highly scalable